What is claimed is:

1. A fast Fourier transform device and comprising:

an FFT/IFFT unit constituted with one hardware, for performing a fast Fourier transform (FFT) and an inverse fast Fourier transform (IFFT); and

a control signal input unit for outputting a control signal for controlling an operation of the FFT/IFFT unit.

2. The device of claim 1, further comprising:

a convergent block floating point (CBFP) for compensating quantization noise generated from the FFT/IFFT unit; and

a read only memory (ROM) for storing twiddle factors used in the FFT/IFFT unit as a table form.

3. The device of claim 1, wherein the FFT/IFFT unit performs an IFFT at the time of transmitting a signal, and performs an FFT at the time of receiving the signal.

4. The device of claim 1, wherein the FFT/IFFT unit is realized by a pipelined method which enhances an operation speed of data.

5. The method of claim 1, wherein the control signal input unit outputs a reset signal for initializing the FFT/IFFT unit, an FFT/IFFT mode determination signal for determining the FFT/ IFFT, and a start signal denoting a start of input data.

6. A fast Fourier transform device comprising:

an FFT/IFFT unit constituted with first, second, and third stages respectively including a butterfly for performing a butterfly operation and a complex multiplier for multiplying data outputted from the butterfly by twiddle factors and thus outputting the multiplied value and for performing an FFT/IFFT; and

a control signal input unit for controlling an operation of the butterfly and the complex multiplier of the FFT/IFFT unit and thus outputting a control signal for performing the FFT or the IFFT to the FFT/IFFT unit.

7. The device of claim 6, wherein the first and second stages comprise:

a commutator for aligning input data as a corresponding alignment method;

a butterfly for performing a Radix-4 butterfly operation for data outputted from the commutator; and

a complex multiplier for multiplying data outputted from the butterfly by twiddle factors and thus outputting.

8. The device of claim 6, wherein the third stage comprises:

a commutator for aligning input data as a corresponding alignment method; and

a butterfly for performing a Radix-4 butterfly operation for data outputted from the commutator.

9. The device of claim 6, further comprising:

a convergent block floating point (CBFP) for compensating quantization noise generated from the FFT/IFFT unit; and

a read only memory (ROM) for storing twiddle factors used in the FFT/IFFT unit as a table form.

10. The device of claim 6, wherein the FFT/IFFT unit performs an IFFT at the time of transmitting a signal, and performs an FFT at the time of receiving the signal.

11. The device of claim 6, wherein the FFT/IFFT unit is realized by a pipelined method which enhances an operation speed of data.

12. The method of claim 6, wherein the control signal input unit outputs a reset signal for initializing the FFT/IFFT unit, an FFT/IFFT mode determination signal for determining the FFT/ IFFT, and a start signal denoting a start of input data.